REMARKS

Claims 1-9 and 16-31 are pending in the present application. Claims 10-15 have been previously withdrawn pursuant to a Restriction Requirement. By this Response, claims 1, 2, 20 and 21 have been amended and claims 29-31 are new. Reconsideration and allowance are respectfully requested.

I. Claim Rejections

Claims 1-9 and 16-28 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,055,630 to D'Sa et al. Applicants traverse this rejection and respectfully assert that D'Sa does not disclose all of the claimed limitations.

With specific regard to claims 1, 16 and 20, D'Sa fails to provide for determining *at a decoder* whether a resume condition is present as claimed. Rather, D'Sa teaches that the "*trace cache unit* 130 snoops the instruction path 122 (between allocation unit 140 and instruction pool 141)" (emphasis added), and that "[i]f trace cache unit 130 recognizes that an instruction originating from IFU 110 corresponds to the first instruction in an instruction trace segment (a 'trace head'), i.e., a trace cache hit... trace cache unit 130 provides the appropriate instructions to allocation unit 140 from its cache memory" (see col. 6, lines 25-34). Thus, D'Sa's determination occurs at the trace cache 130 and not at the decoder as claimed. As a result, the solution offered by D'Sa is entirely different from the claimed approach.

While the Office Action states that "controlling part of the trace cache unit can be made part of the decoder", Applicants assert that such an interpretation runs contrary to the express teachings of D'Sa, as indicated above. Indeed, it is clear from D'Sa that the "[t]race cache unit 130 controls whether the source for instructions entering instruction pool 141 is instruction fetch unit 110... or trace cache unit 130" (see col. 6, lines 22-24), and that the trace cache unit 130 is the focal point of the snooping process. Simply put, D'Sa neither expressly nor inherently provides for determining at a decoder whether a resume condition is present. For at least the above reasons, claims 1, 16 and 20 are not anticipated by D'Sa.

With further regard to claims 2, 16 and 21, D'Sa fails to provide for switching an allocation module from a decoder reading state to a trace cache reading state as claimed. Rather, D'Sa teaches that in response to a trace cache hit, "trace cache unit 130 signals instruction fetch

unit 110 to discontinue fetching instructions" (see, col. 6, lines 29-31), and makes no mention of switching the reading state of the allocation unit 140.

With further regard to claims 2-9, 17-19 and 21-28, the rejected claims depend from claims 1, 16 and 20, discussed above, and therefore also recite patentable subject matter. Accordingly, Applicants respectfully request that the Examiner withdraw the instant rejection.

II. New Claims

With regard to new claims 29-31, Applicants point out that D'Sa demonstrates no appreciation for determining whether a resume condition is present before a second instruction leaves a decoder as claimed. Accordingly, claims 29-31 also recite patentable subject matter.

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CONCLUSION

Applicants assert that all claims are in condition for allowance. Applicants respectfully request the Examiner to pass this case to issue at the Examiner's earliest possible convenience.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 703.633.0962.

Respectfully submitted,

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